ABSTRACT OF THE DISCLOSURE

A method of processing first and second scheduled packets of real-time information includes computing for each packet a deadline interval and ordering processing of the packets according to the respective deadline intervals. A single-chip integrated circuit has a processor circuit and embedded electronic instructions forming an egress packet control establishing an egress scheduling list structure and operations in the processor circuit that extract a packet deadline intervals, place packets in the egress scheduling list according to deadline intervals; and embed a decoder that decodes the packets according to a priority depending to their deadline intervals.